

REV	ECN NO.	DISCRIPTION	CHEKED/DATE	APPD/DATE

NOTES: 1.MATERIAL:
MOLDING: LCP UL94 V-0
CONTACT:COPPER ALLOY.
GOLD PLATED Min ON CONTACT AREA,100u''
Min TIN (LEAD FREE) ON SOLDER AREA,
SHELL: SUS304-H,T=0.30±0.03mm
50u'' NICKEL PLATING OVER ALL.
SHILD:SUS304-H,T=0.12±0.03mm

2.MECHANICAL:
INSERTION: 5~20N.
EXTRACTION: 8~20N AFTER TEST.
DURABILITY: 10000 CYCLES

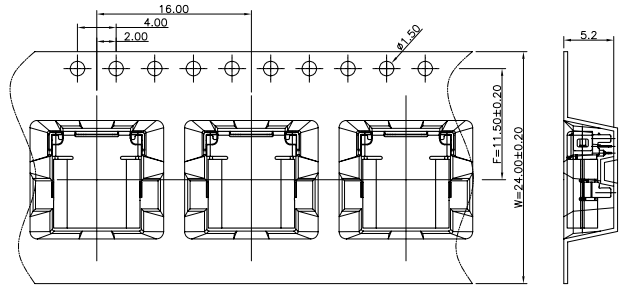
3.ELECTRICAL:
CURRENT: 5A FOR VBUS;
1.25A FOR GND PIN.
0.25A FOR OTHER.
VOLTAGE: 20 V MAX
WITHSTANDING VOLTAGE: 100V AC R.M.S.
CONTACT RESISTANCE: 40mΩ MAX.
INSULATION RESISTANCE: 100MΩ MIN.

4.ENVIRONMENTAL
TEMPERATURE RANGE -25°C ~ +85°C

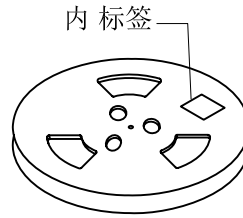
H D C 有限公司

.X:±0.25	X.:±1°	APP.	DWG NO.	UC-010-03
.XX:±0.15	.X:±0.5°			
.XXX:±0.05	.XX:±0.02°	CHK.	TITLE	USB 3.1 C TYPE DIP+SMT母座 四脚插板 8.65L
UNIT mm		DGN. 15.10.20		
SCALE 1:1		DRW. 15.10.20	SERIES	
REV. A0	SHEET: 1/1			

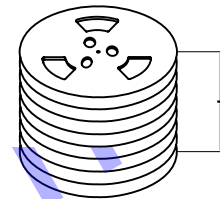
REV	ECN NO.	DISCRIPTION	DRAWN/DATE	CHEKED/DATE	APPROVED/DATE



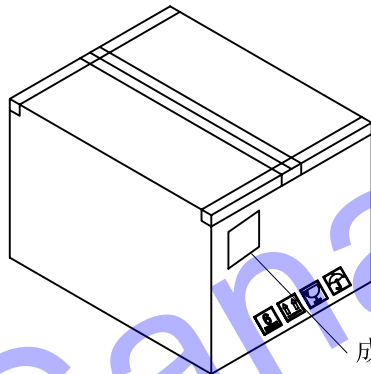
① 产品入载带示意图



② 卷盘贴标签示意图

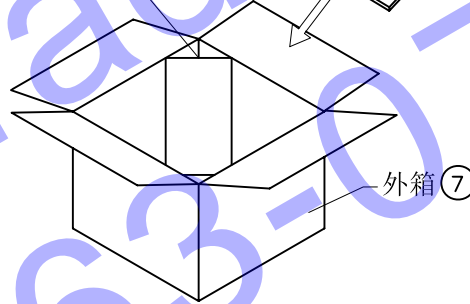


③ 10盘产品叠层示意图



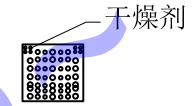
⑥ 外箱封箱示意图

⑥ 三角套(4pcs)



⑤ 产品入外箱示意图

⑤ 纸板(2pcs)
分别放在外箱底面
和最上面



④ 10盘产品入防水袋示意图

封口面
防水袋封口面朝上

包装说明:

1. 将检验好的成品;SMT朝下放入载带底部;每卷装1000PCS产品;具体如图一所示
2. 将包装好的产品;每盘必需贴上内标签;具体如图二所示
3. 将贴好内标签的产品每8盘叠一层装入防水袋中并加一包干燥剂;装好后将防水袋封好;具体如图三四所示
4. 先将1pcs平卡放入纸箱底部;然后将装好产品的防水袋装入纸箱中;防水袋热熔封口,封口面需朝上;并将4PCS三角套分别装入4个角;如图五所示
5. 装好后将1pcs平卡放入纸箱最上面并封好纸箱及贴好相关标签;具体如图六所示;(产品包装的标签,如客户有要求,请按客户要求包装出货)
6. 载带前面留30PCS空格,后面留20PCS空格
7. COVER与CARRY剥离力:50-125g,速度:300mm/分钟左右,剥离角度:165°-180°

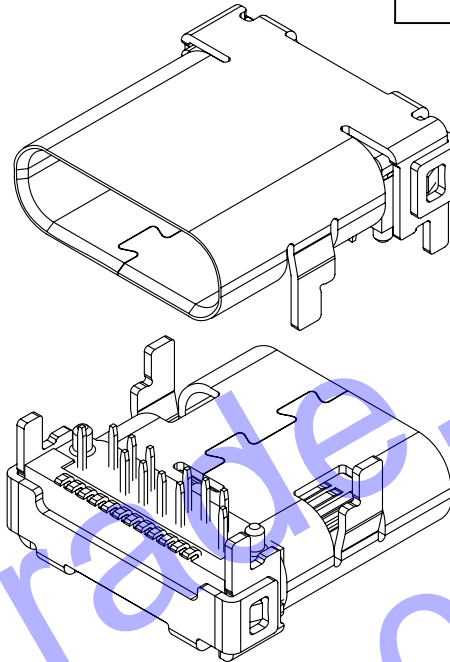
图四

图三

H D C 有限公司

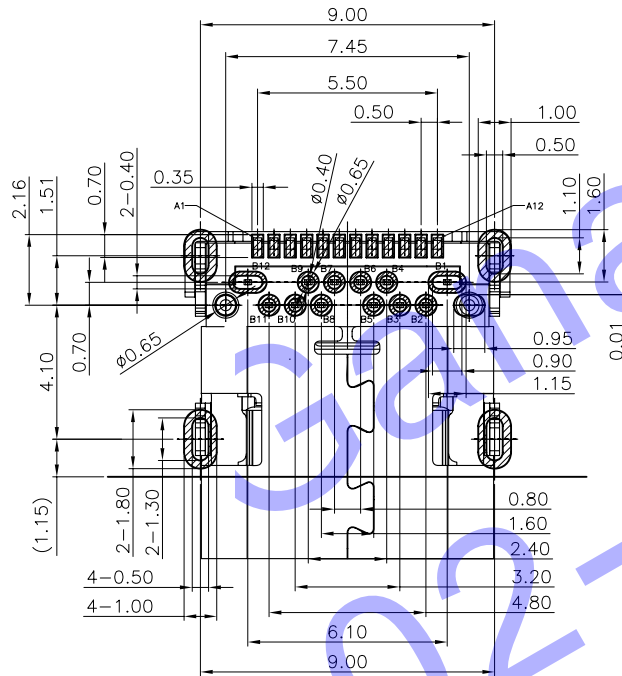
.X :±0.50	X. :±1'	APP.		PART NO	
.XX :±0.30	.X :±0.5'	CHK.		TITLE	USB 3.1 C TYPE母座卷装图
.XXX:±0.25	.XX:±0.02'	DGN.	2015.09.20	SERIES	
UNIT	mm	DRW.	2015.09.20		
SCALE	1:1				
REV.	A0	SHEET:	1/1		

D		E	F
REV	ECN NO.	DISCRIPTION	CHEKED/DATE APPD/DATE



USB TYPE-C FULL-FEATURED RECEPTACLE INTERFACE PIN ASSIGNMENTS

PIN	Signal Name	Description	PIN	Signal Name	Description
A1	GND	Ground return	B12	GND	Ground return
A2	SSTXp1	Positive half of first SuperSpeed TX differential pair	B11	SSRXp1	Positive half of first SuperSpeed RX differential pair
A3	SSTXn1	Negative half of first SuperSpeed TX differential pair	B10	SSRXn1	Negative half of first SuperSpeed RX differential pair
A4	VBUS	Bus Power	B9	VBUS	Bus Power
A5	CC1	Configuration Channel	B8	SBU2	Sideband Use (SBU)
A6	Dp1	Positive half of the USB 2.0 differential pair-Position 1	B7	Dn2	Negative half of the USB 2.0 differential pair-Position 2
A7	Dn1	Negative half of the USB 2.0 differential pair-Position 1	B6	Dp2	Positive half of the USB 2.0 differential pair-Position 2
A8	SBU1	Sideband Use(SBU)	B5	CC2	Configuraation Channel
A9	VBUS	Bus Power	B4	VBUS	Bus Power
A10	SSRXn2	Negative half of second SuperSpeed RX differential pair	B3	SSTXn2	Negative half of second SuperSpeed TX differential pair
A11	SSRXp2	Positive half of second SuperSpeed RX differential pair	B2	SSTXp2	Positive half of second SuperSpeed TX differential pair
A12	GND	Ground return	B1	GND	Ground return



RECOMMEND P.C.B LAYOUT(COMPONENT SIDE)

TOLERANCE FOR PCB LAYOUT IS ± 0.05

KEEP OUT AREA

H D C 有限公司

.X:±0.25	X.:±1°	APP.	DWG NO.	UC-010-03
.XX:±0.15	.X:±0.5°			
.XXX:±0.05	.XX:±0.02°	CHK.	TITLE	USB 3.1 C TYPE R/A SMT PCB LAYOUT
UNIT mm		DGN.		
SCALE 1:1		DRW.	15.09.20	SERIES
REV. A0	SHEET: 2/2			